

**THAT WHICH IS CLAIMED IS:**

1. Device for processing interruptions in a Slave apparatus (B) such as a computer peripheral which is connected to a Master apparatus (A) such as a computer via a cable (20) having several conductors to enable an exchange of binary information between the two apparatuses according to the USB protocol, said 5 Slave apparatus comprising:

a sending/receiving circuit (24) for binary information received and sent over the cable (20),  
10 which supplies signals (Setup, CTR, End\_trans),  
control circuit means (30R, 30T, 50R, 50T)  
for controlling state latches (32R0/32R1, 32T0/32T1,  
52R, 52T) receiving the signals (Setup, CTR, End\_trans)  
15 of the sending/receiving circuit (24) and supplying  
state signals of the sending/receiving circuit, and  
a microcontroller (28) for processing  
applications of the Slave apparatus and, notably, the  
binary information received and sent over the cable  
(20), via the sending/receiving circuit, characterized  
20 in that said interruption processing device comprises a  
control circuit (80) for controlling an interruption  
state latch (70) such as to supply an interruption  
signal (SOVR) when the sending/receiving circuit (24)  
has received the start (SETUP) of a new message, said  
25 start of message having been acknowledged (ACK) and  
recorded by said sending/receiving circuit.

2. Device according to claim 1,  
characterized in that said control circuit for  
controlling the interruption state latch (70) comprises  
logic circuits (74, 76 and 78) which, receiving the  
5 signals (Setup, End\_trans, CTR) of the  
sending/receiving circuit (24), supply a signal  
(Setupovr) which sets the interruption state latch to a

"1" state to indicate a microprocessor interruption request.

3. Device according to claim 1 or 2, characterized in that the control circuit means for controlling the state latches (32R, 32T, 52R and 52T) further comprise means (42, 62) for preventing writing 5 into the state latches (32R0/32R1, 32T0/32T1, 52R and 52T) by the microprocessor (28) during the receipt of a start of message (Setup) and the presence of the interruption signal (SOVR).

4. Method of processing interruptions in a Slave apparatus (B), such as a computer peripheral, which is connected to a Master apparatus (A), such as a computer, by a cable having several conductors capable 5 of operating according to the so-called "USB" protocol, characterized in that it comprises the steps of:

- (a) producing a state signal (CTR) indicating the end of a message,
- (b) detecting the start (16) of a new message 10 coming from the Master apparatus and producing a start of message state signal (Setup),
- (c) recording the data contained in said start of message,
- (d) acknowledging receipt (ACK) of said start 15 of message,
- (e) producing a signal (End\_trans) indicating the end of the previous step (c), and
- (f) producing an interruption signal (SOVR) in the presence of signals signaling an end of 20 preceding message (CTR), a start (Setup) of a new message and the end of step (e) (End\_trans).